REMARKS

The present application was filed on January 5, 2004 with claims 1 through 42. Claims 38-42 were cancelled in the Amendment and Response to Office Action dated December 13, 2005. Claims 1 through 37 are presently pending in the above-identified patent application. Claim 1 and 21 are proposed to be amended herein. A typographical error in the specification is also corrected.

In the Office Action, the Examiner has requested that a prior art label be added to Figures 1B, 2B, 4B, 5B, and 6-9. The Examiner rejected claim 12 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement, objected to claim 32 due to indicated informalities, and rejected claims 1, 2, 9-16, 21-23, and 29-35 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner also rejected claims 1-2, 9-10, 13-15, 21, 23, 31, and 35 under 35 USC 102(b) as being anticipated by Mead et al. (United States Patent No. 5,844,265), and rejected claim 11 under 35 U.S.C. §103(a) as being unpatentable over Mead et al., and in view of Ravi et al. (United States Patent Application Publication Number 2004/0263272 A1) and Brachitta et al. (United States Patent Number 6,130,469). The Examiner indicated that claims 3-8, 17-20, 24-28, and 36-37 are allowed. Applicants acknowledge with deep gratitude the Examiner's indication that the application contains allowable subject matter.

Formal Objections

Drawings

The Examiner has requested that a prior art label be added to FIGS. 1B, 2B, 4B, 5B, and 6-9.

In the Amendment and Response to Office Action dated December 13, 2005, Applicants labeled FIGS. 2B, 5B, 7 and 9 as "prior art" in accordance with the Examiner's suggestion and each sheet was labeled as a "Replacement Sheet."

With regard to FIGS. 1A, 1B, 1C, 4A, 4B, 6 and 8, Applicants submit that

FIGS. 1A, 1B, 1C, 4A, 4B, 6 and 8 show a gated diode structure with only a gate and a source (and no drain). There are only two terminal areas for the gated diode. The present invention recognizes that this structure without the drain leads to significantly smaller gated diode physical structure (which keeps the area much smaller in applications such as memories and sense amplifiers). Thus, FIGS. 1B, 4B, 6 and 8 are different from what is shown by the prior art, including Mead. With regard to the Examiner's references to passages in the specification in the March 1, 2006 Office Action, applicants respectfully note that the terminology "conventional" on line 10 of page 8 is best understood as modifying "FET", not as any admission as to prior art status of material depicted in the pertinent figures; that is, "conventional" FETs can be modified by the teachings of the present invention to obtain the depicted inventive structures. Accordingly, applicants respectfully submit that the substitute formal drawings submitted on Dec. 13, 2005 have already responded to the Examiner's objection as to FIGS. 2B, 5B, 7 and 9, and that the objection as to FIGS. 1A, 1B, 1C, 4A, 4B, 6 and 8 is inappropriate for the reasons set forth herein. Note that two typographical errors in the paragraph beginning at page 8 line 10 are corrected herein (- - Transistor - - substituted for "Transformer", support being found throughout the specification, for example, at page 8, line 3; and - - and - - being substituted for "an", the intent of the original passage being apparent).

Claim 32 was objected to because there is insufficient antecedent basis for the limitation "the step."

Applicants note that claim 32 is dependent on claim 21, and that claim 21 requires a modifying voltage step. Thus, the limitation "the step of modifying voltage" in claim 32 refers to the modifying voltage step in claim 21 and has proper antecedent basis.

Applicants respectfully request that the objections to the drawings and claim 32 be withdrawn.

Claims 1, 3, 4, 6, 16, 21, 22 and 24

In the Amendment and Response to Office Action dated May 18, 2006, Applicants indicated that claims 1, 3, 4, 6, 16, 21, 22, and 24 have been amended to

require first, second, third, and fourth voltage ranges. As noted by the Examiner, the cited amendments require only first and second voltage ranges. Applicants apologize for any confusion.

Section 112 Rejections

Claim 12 is rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement, and claims 1, 2, 9-16, 21-23, and 29-35 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding claim 12, the Examiner asserts that the cited gated diode is actually a one-terminal device because the source/drain and gate are short-circuited. Regarding claims 1, 2, 9-16, 21-23, and 29-35, the Examiner asserts that the gated diode is "in itself not adapted while a function either is there inherently or is not," and asserts that the "newly added limitation thus raises the question whether 'adapted' refers to the device or to its function and if to its function whether merely by placement within the integrated circuit."

Regarding claim 12, Applicants note that the cited claim requires wherein the two terminal semiconductor device comprises a gated diode comprising an insulator formed between a gate and a well, a source diffusion region abutting and overlapping one side of the insulator and gate, a drain diffusion region abutting and overlapping another side of the insulator and gate, and a coupling that electronically couples the source and drain regions, wherein the second terminal is coupled to the source diffusion region and the first terminal is coupled to the gate. Applicants find no requirement in claim 12 that the source/drain and gate are short-circuited.

Regarding claims 1, 2, 9-16, 21-23, and 29-35, Applicants note that claim 1 has been amended to delete the limitation "wherein the two terminal semiconductor device is adapted to amplify said signal in response to a substantial change in voltage of said control signal," and claim 21 has been amended to recite "wherein the two terminal semiconductor device amplifys said signal in response to a substantial change in voltage

of said control signal." Applicants believe that these amendments address the Examiner's concerns and respectfully request that the section 112 rejections be withdrawn.

Prior Art Rejections

Claims 1-2, 9-10, 13-15, 21, 23, 31, and 35 were rejected under 35 USC 102(b) as being anticipated by Mead et al. The Examiner asserts that Mead discloses a circuit 10 for amplifying signals, a control line (LOAD BIAS connected to a bias voltage source); and a two terminal semiconductor device 62-1 (MOS transistor used as varactor with source and drain short-circuited), having first and second terminals, the first terminal (gate of gated diode 62-2) coupled to a signal line 194-1 (of sense amplifier 10), and the second terminal coupled to the control line (capacitively, through 16-1). The Examiner further asserts that Mead discloses wherein the two-terminal semiconductor device is CAPABLE of amplifying said signal in response to a substantial change in voltage of said control signal. The Examiner asserts that Applicants admit that any amplifying function is inherent as a property of capability of said gated diode. The Examiner asserts that, in reference to the claim language referring to "wherein the two-terminal semiconductor device is adapted to amplify," intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. Finally, the Examiner asserts that the limitation "adapted" pertains itself to a method of making the device and as such constitutes a product-by-process limitation.

Mead does not teach a varactor utilized for performing amplification.

Initially, it is noted that the varactors (62-n) of Mead are not even used for signal amplification. Rather, Mead teaches that the "(u)se of a varactor structure allows ***compression*** *of the output signal* over a wide dynamic range of input signals." (See, col. 3, lines 25 – 26; emphasis added.) Applicants also note that Mead teaches that

> another object of the present invention is to provide an

> integrated photosensing imager system including a sense amplifier having low noise, low power dissipation, and a ***compressive input-output characteristic*** such that it will decrease its gain gradually at large inputs rather than clip abruptly and which can fit into the width of a single pixel in a photosensor array.
> (Col. 1, lines 47-53; emphasis added.)

Mead also teaches that

> a balance transistor 30, shown as a P-C-Channel MOS transistor, is connected between input line 18 and output node 28, and has its gate connected to a BAL signal node 31. In addition, as presently preferred, a varactor structure 32 may be connected between the input and output of amplifier 10. Use of a varactor structure *allows* ***compression*** *of the output signal over a wide dynamic range of input signals*.
> (Col. 3, lines 20-26; emphasis added)

Thus, Mead teaches that the varactor ***compresses*** *signals*; Mead does *not* disclose or suggest that the varactor *amplifies signals*

Mead does not teach a two-terminal device for performing amplification.

The Examiner is asserting that the three terminal MOS transistors 62-1 through 62-4 in FIG. 7 of Mead are two terminal devices, because the source and drain of the transistors 62-n are short circuited. Assuming for the sake of argument that the transistors 62-1 through 62-4 with connected source and drain are two terminal devices, Mead still does not teach at least one a number of other limitations of the independent claims. The present invention does not claim a two-terminal structure by itself. Rather, *each independent claim explicitly recites connecting such two-terminal devices in a certain way to perform signal amplification*.

Mead does not teach an amplification control line.

The transistors 62-n of FIG. 7 in Mead, such as transistor 62-1, are connected between a LOAD BIAS (the Examiner is calling this the control line) and first sense line 194-1 (the Examiner is calling this the signal line).

First, the transistors 62-n in FIG. 7 are not directly connected to the

LOAD BIAS, but rather are connected to the LOAD BIAS via the output signal (not numbered in FIG. 7 of Mead, but numbered as OUT or 28 in FIG. 1 of Mead). It is noted that the LOAD BIAS is a DC voltage to bias the amplifier which comprises the transistors 12, 14 and 16 in FIG. 1 (often referred to as a cascode amplifier), and is not a control line as defined in the art and as would be well understood by a person of ordinary skill in the art. Both independent claims 1 and 21 require that "*the second terminal (is) coupled to the* ***control line***."

Assuming, for the sake of argument, that one even considers the LOAD BIAS as a control line, the varactors (62-n) are not coupled to a control line. Indeed, it is coupled or directly connected to the output of the amplifier which is clearly a signal, numbered as OUT or 28 in FIG. 1 of Mead). Further, in column 3, lines 23 - 25 of Mead, it is noted that "... a varactor may be connected between the input and output of amplifier." The input and output of an amplifier are signals, which cannot be considered as a control line, as defined in the context of the present invention.

Applicants also note that Mead teaches that

> the drain of cascode transistor 14 is connected to the drain of load transistor 16. The source of load transistor 16 is connected to ground rail 24 and the gate of load transistor 16 is connected to load bias node 26. *Load bias node 26 is connected to a bias voltage source* ***supplying a load bias voltage well above the threshold voltage*** *of the transistor.* The output node 28 of amplifier 10 is the common connection of the drains of cascode transistor 14 and load transistor 16
> (Col. 3, lines 10-18; emphasis added.)

Claim 1 has been amended to require a *coupling element coupled to the control line and a control signal, wherein said coupling enables said control signal to* ***control an amplification***, and claim 21 has been amended to require *wherein the two terminal semiconductor device* ***amplifys said signal in response to a substantial change in voltage of said control signal***. As noted above, Mead does ***not*** disclose or suggest a *coupling element coupled to a control line and a control signal, wherein said coupling enables the control signal to control an amplification,* Mead does ***not*** disclose or suggest

that the varactor is *adapted to amplify a signal,* and does ***not*** disclose or suggest a *substantial change in voltage of a control signal.*

Thus, Mead does ***not*** disclose or suggest that "the second terminal (is) coupled to the control line," does ***not*** disclose or suggest a *coupling element coupled to the control line and a control signal, wherein said coupling enables said control signal to control an amplification,* as required by independent claim 1, as amended, and does ***not*** disclose or suggest *wherein the two terminal semiconductor device amplifys said signal in response to a substantial change in voltage of said control signal,* as required by independent claim 21, as amended.

Regarding the Examiner's assertion that the limitation "adapted" pertains itself to a method of making the device, that said disclosed gated diode "is in itself not adapted while a function is either is there inherently or is not," that "the process of adaptation itself has no patentable weight in the product invention while only the capability of performing an amplification function is of patentable weight, not the amplification process itself, in as far as claim 1 is concerned," and that, in reference to the claim language referring to "wherein the two-terminal semiconductor device is adapted to amplify," intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art, Applicants note that the cited use of the term "adapted" has been deleted from the cited claims.

Regarding the Examiner's assertion that "only the capability of performing an amplification function is of patentable weight, not the amplification process itself, in as far as claim 1 is concerned," Applicants note that the circuit disclosed by Mead is ***not*** *capable of an amplification function since the LOAD BIAS signal is a DC voltage and* ***not*** *a control signal that can control the amplification function.*

Applicants respectfully request that the rejection under section 102 be withdrawn.

Dependent Claims

The Examiner has already indicated that claims 3-8, 17-20, 24-28, and 36-37 are allowed. The remaining dependent claims are dependent on independent claims 1 and 21, and are therefore patentably distinguished over Mead because of their dependency from amended independent claims 1 and 21 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

All of the pending claims following entry of the amendments, i.e., claims 1-37, are in condition for allowance and such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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